

Examination August 21, 2007

Physical electronics, EMI180

Examination occurs Tuesday August 21 between 08.30 och 12.30.
Responsible teacher: Per Lundgren, tel. 772 18 82.

Solutions will be posted on the course homepage (EMI180) Wednesday August 22.

Preliminary results will be available on the course homepage no later than Wednesday 7/9, and examination of the results is possible on the same day between 10-12 at MC2 (room B509).

The problems can be solved using the tools of your choice excluding personal interaction and excluding internet access. Select *only* three of the four problems to treat and hand in solutions to these three. In order to pass two of the three solutions must show that you are able to apply concepts/models/methods from the course on a problem in a sensible manner (grade 3).

The solutions will be graded either fail, 3, 4 or 5.

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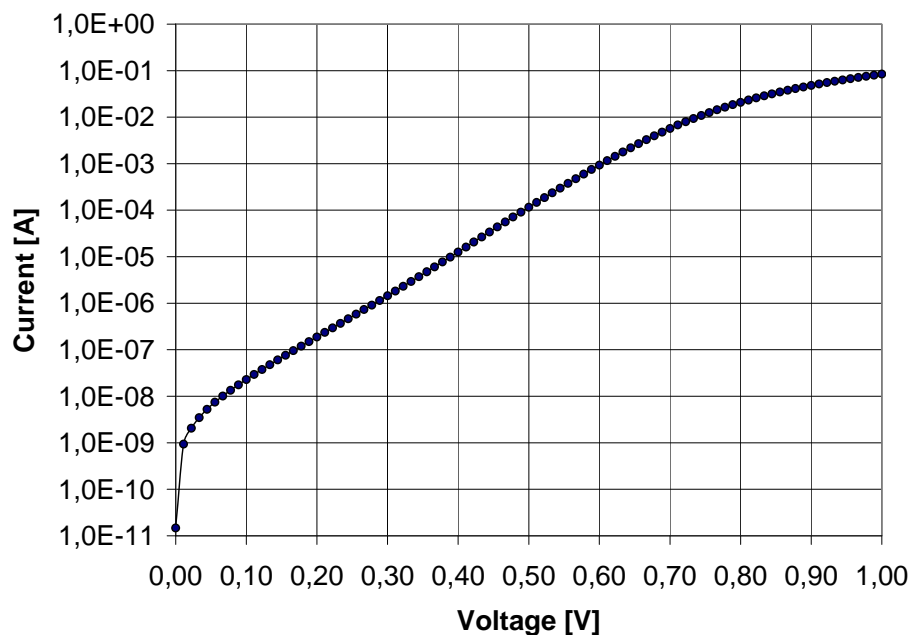
August 2007

Problem 1

In the appended paper (“Vertically standing carbon nanotubes as charge storage nodes for an ultimately scaled nonvolatile memory application”, Seong-Wan Ryu et al., Applied Physics Letters 91, 2007), the authors present the transfer characteristics of two different MOSFETs with “floating gates” made up of carbon nanotubes. Unfortunately they have omitted information on what drain-source voltage they have employed for these measurements. Make a quantitative estimation of what drain-source voltage they are likely to have used!

Problem 2

First give a model for the room temperature device characteristics in the figure below. This model is to be used to predict the current to within $\pm 20\%$ for the voltage range between 0,1 and 0,7 V and it should be as simple as possible. Then make a motivated suggestion for an extended model for the current for negative voltages down to -10 V for this device. Thus both positive and negative voltages must be treated for grade 3 (or higher)!



Problem 3

Your spacecraft has been damaged in an accident. In order for you to be able to bypass an electronic jam and run your emergency propellant system manually, you need to plug in an electronic thermometer (thermistor) which needs to show a resistance higher than 1 M Ω for temperatures below 400 K and drop down to a value below 1 k Ω for temperatures above 700 K. It needs to operate in the temperature range from 100 K up to 800 K. Suggest a scheme to make a “home made” device to fulfil these requirements using some surviving standard semiconductor based electronics from the end of the 20th century in your electronics workshop and explain what physical mechanism you base your device functionality on. Which are the weakest links in your design suggestion?

Problem 4

You are investigating a novel semiconducting material to use for low-cost digital electronics. It is possible to design both n-channel and p-channel FETs in this material and you want to build complementary logic gates, like silicon CMOS. For the n-channel devices you can describe the current-voltage characteristics with an empirical model as follows:

$I_D = 4 \cdot V_{DS} \cdot (V_{GS} - V_T) \cdot W$, where W is the width of the transistor, which can be chosen from 1 μm up to 1 mm. The threshold voltage, V_T , is 0 V.

For the p-channel devices the empirical model gives:

$I_D = 0,1 \cdot V_{DS} \cdot (V_T - V_{GS}) \cdot W$. In this case the threshold voltage is 1 V; thus it is a depletion mode transistor.

Demonstrate if you can design a complementary inverter using these devices in a circuit with a maximum voltage of 5 V.

Suggested solutions

These suggested solutions are unfortunately NOT designed model suggestions for any particular grading, but simply brief descriptions of one possibility of dealing with the problems in a sensible manner.

Problem 1

Looking at figure 2 in the paper, we see that the transfer characteristics for the two different devices look quite similar. I presume that the authors have used the same drain-source voltage in both cases, but here is room for criticism towards the authors: they have not clearly stated that the measurement conditions are the same for both devices, so the similarity between the devices could be an artefact. In order to determine the value of the drain-source voltage they have employed I start by checking what current we would expect from these devices if they were biased in saturation, i. e. with a drain-voltage high enough so that the current can be expressed by e. g.:

$$I_{DSAT} = \frac{W}{L} C_{OX} \mu \frac{1}{2} (V_{GS} - V_T)^2.$$

From figure 2 we can infer that the threshold voltage is close to 0 V. The ratio of width to length is given as 25. We can assume that the (electron) mobility is similar as that of other average n-channel MOSFETs, i. e. takes a value of about 0.05 m²/Vs. Since we have a complex region of mixed insulators and carbon nanotubes between the channel and the gate, it is not trivial to calculate the oxide capacitance per unit area, C_{ox} . With the assumption that the carbon nanotubes are perfect conductors (and in a more or less flat layer), we can model the capacitance as consisting of two capacitors in series: one 30 nm thick with a dielectric constant of 25, and one 4.5 nm thick with a dielectric constant of 4. The net oxide capacitance will then be:

$$C_{OX} = \left(\frac{1}{C_{SiO2}} + \frac{1}{C_{HfO2}} \right)^{-1} \approx 4 \cdot 10^{-3} \frac{F}{m^2}.$$

Putting all the values together to calculate I_{DSAT} , we end up with a current of about 10 mA at a gate voltage of about 5 V. In figure 2 in the paper we see that the measured drain current is limited to less than 0.5 mA – more than one order of magnitude smaller than our calculated saturation current. (The current in the figure is given as current per unit channel width). It is fairly obvious that the drain voltage needs to be quite small to obtain this low value, so we employ a current expression for small drain-source voltages instead:

$$I_D = \frac{W}{L} C_{OX} \mu (V_{GS} - V_T) V_{DS},$$

and from this we obtain $V_{DS} \approx 20$ mV.

Problem 2

An ideal diode curve that would fit looks like:

$$I = 2.5 \cdot 10^{-9} e^{21 \cdot V} \text{ A.}$$

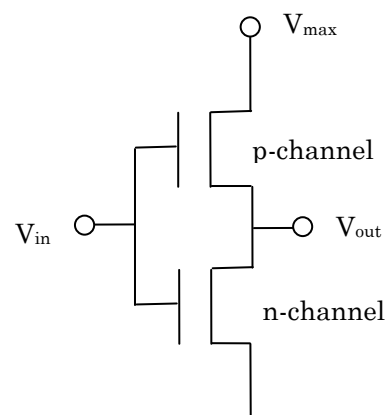
Assuming that we indeed are dealing with a (silicon) pn-junction diode, the exponent is far from qV/kT , which tells of a diode with a strong contribution of recombination in the forward direction. We thus expect a strong generation contribution in the reverse direction, and can surmise that the doping is low (wide depletion layer) and the breakdown voltage high. The voltage dependence is likely to be weak (square root of voltage), so down to -10 V I suggest a simple approach of a constant negative current of the same order as the saturation current ($-3 \cdot 10^{-9}$ A).

Problem 3

The weakest link will probably be contacts and a design that withstands the high temperatures for the contacts. In principle I would try to dig out connections/access to chip substrates (which have a relatively low doping level) and exploit the fact that the semiconductor (silicon) will turn intrinsic at higher temperatures, which will give a sharp decrease in resistance.

Problem 4

First I note that there is severe asymmetry in the devices, which however can partly be designed away by choosing different widths for the p- and n-channel transistors. I therefore choose a p-channel width that is 40 times larger than the n-channel width, lets say $1 \mu\text{m}$ n-channel and $40 \mu\text{m}$ p-channel. The inverter circuit will look like:



V_{max} is 5 V. For an input voltage of 5 V, we can find the output voltage by demanding that the current through the transistors must be equal (infinite load impedance), which implies:

$$5 \cdot V_{out} = V_{max} - V_{out} \Rightarrow V_{out} = \frac{5}{6} V.$$

The low output will be almost 1 V. If we have 1 V at the input, the output will be:

$$1 \cdot V_{out} = (V_{max} - V_{out}) \cdot 5 \Rightarrow V_{out} = \frac{5}{6} V_{max}.$$

It looks like we have OK inverting action in one inverter. One drawback compared to CMOS is that we will have quite some current flowing through the transistors. Another drawback is that we cannot connect too many inverters (or similar gates) after one another, since each gate makes the output approach the limiting value that gives the same output as input voltage:

$$V_{out}^2 = (V_{max} - V_{out}) + (V_{max} - V_{out})^2 \Rightarrow V_{out} \approx 2.7 V.$$